

Scale of Integration

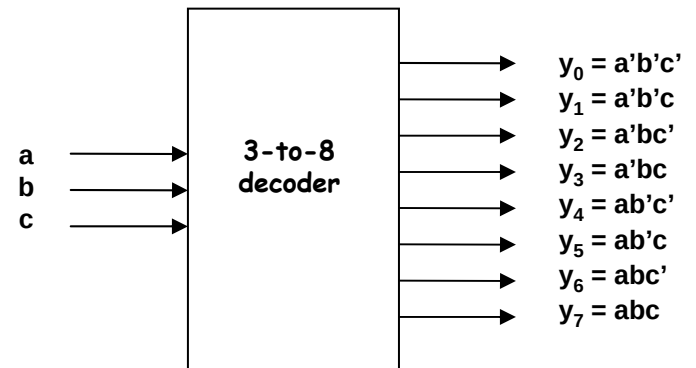
Integration	Types of circuits	Size
SSI	Inverters Gates Flip -Flops	1 to 4 Gates 6 Inverters 1 to 2 Flip -Flops
MSI	Multiplexers Decoders Registers, Counters Adders	12 to 100 Gate Equivalents
LSI	Small Memories Small Microcontrollers	100 to 3000 Gate Equivalents
VLSI	Memory PC Processor	More than 3000 to 5000 Gate Equivalents

Binary Decoder

- A binary code of N bits is capable of representing up to 2^N distinct elements of coded information.
- A decoder is a combinational circuit that converts binary information from N input lines to up to 2^N output lines. These decoders are called N -to- M line decoders such that: $M \leq 2^N$
 - Binary decoder has N inputs and 2^N outputs
 - All 2^N minterms are generated

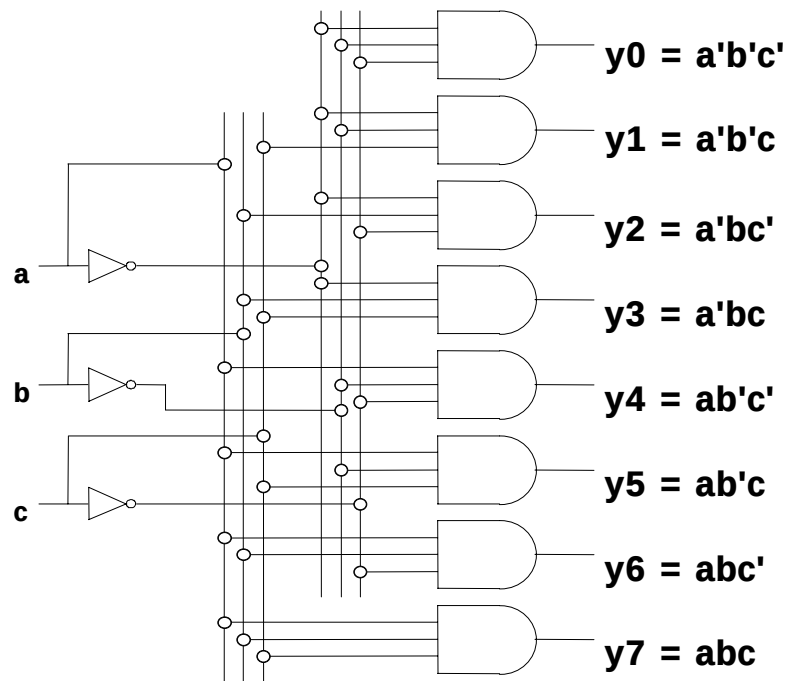
Example: 3-to-8 decoder

A 3-to-8 line decoder has three inputs and eight outputs. The decoder decodes the input binary code represented by the three bits and generates all eight minterms of the inputs. Only one output is one while the other seven are zeros.



Binary Decoder

The 3-to-8 decoder can be implemented using three inverters and eight AND gates as shown below:

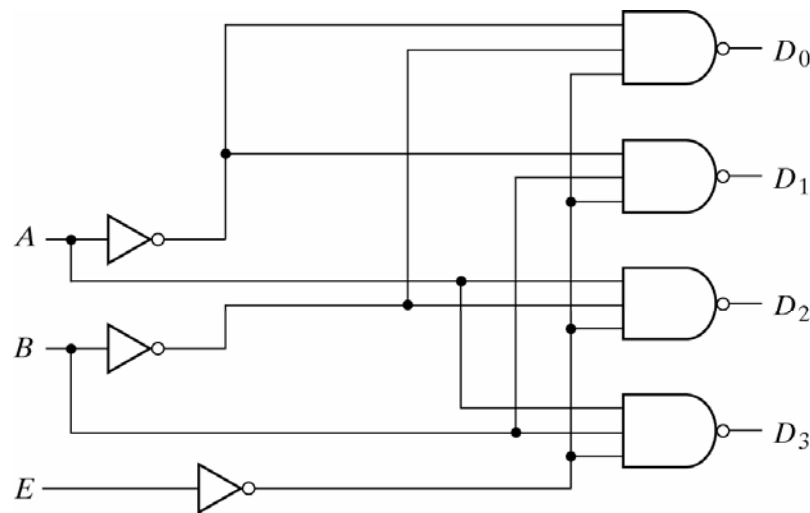


The truth table for the decoder is shown below:

a	b	c	y_0	y_1	y_2	y_3	y_4	y_5	y_6	y_7
0	0	0	1	0	0	0	0	0	0	0
0	0	1	0	1	0	0	0	0	0	0
0	1	0	0	0	1	0	0	0	0	0
0	1	1	0	0	0	1	0	0	0	0
1	0	0	0	0	0	0	1	0	0	0
1	0	1	0	0	0	0	0	1	0	0
1	1	0	0	0	0	0	0	0	1	0
1	1	1	0	0	0	0	0	0	0	1

Binary Decoders with Enable Input

- If we use NAND gates to construct the decoder then the outputs are inverted.
- Decoders are also constructed with one or more enable inputs.
- An example is shown for the 2-to-4 line decoder.



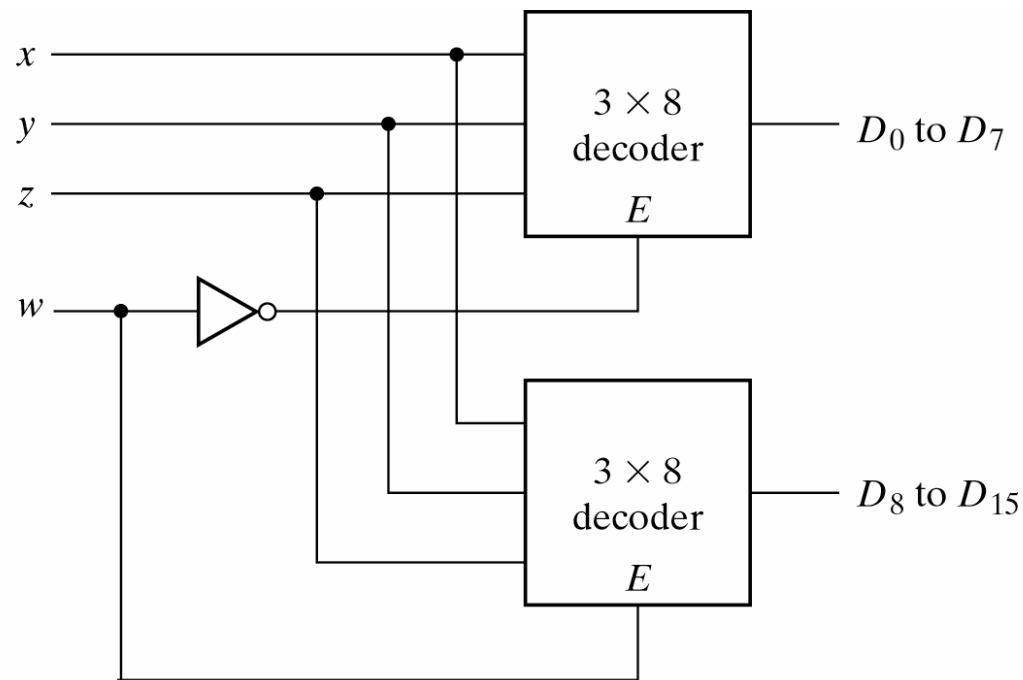
(a) Logic diagram

E	A	B	D_0	D_1	D_2	D_3
1	X	X	1	1	1	1
0	0	0	0	1	1	1
0	0	1	1	0	1	1
0	1	0	1	1	0	1
0	1	1	1	1	1	0

(b) Truth table

Design of Larger Decoders

- A 4 X 16 decoder can be constructed from two 3 X 8 decoders with enable inputs as shown below:

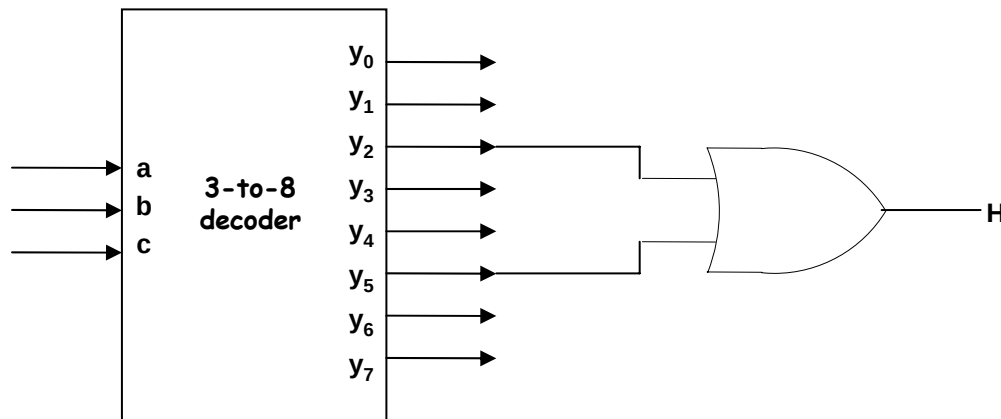


Implementing Logic Functions

- Decoders can be used to implement logic functions.
- Since all the minterms of the function are available at the output then there is no need for simplification.
- All what is needed is an OR gate for each function to sum the required minterms.

Implement:

$$H = ab'c + a'bc'$$



Implement a full adder circuit using an appropriate decoder and OR gates.

The required outputs are:

$$S(x,y,z) = \sum (1,2,4,7)$$

$$C(x,y,z) = \sum (3,5,6,7)$$

